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EXAMINER	
MATTHEW, AARON D	
ART UNIT	**PAPER NUMBER**
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/061,435	KONDO ET AL.
	Examiner	Art Unit
	Aaron D Matthew	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-18,22,23 and 25-39* is/are rejected.

7)☒ Claim(s) *3,19-21,24, and 40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/13/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Fig. 4, element 106. The examiner suggests that said reference character be included with the description on line 31 of page 27, to improve clarity in the disclosure. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

   - The language on lines 18-19 on page 26 is confusing. Examiner suggests changing it to read, "...where an attempt is being made to recover in a controlled manner..."
   - Line 19 on page 27 should be changed to read, "...a two client inquiry message system may be implemented."
   - Line 20 on page 27 should be changed to read, "...messages are used when verifying a particular path..."
   - The step of sending a second inquiry message, indicated on line 31 of page 27, is mislabeled as, "106". The examiner suggests that this reference label be changed to "108" in order to correspond with the associated figure 4.

   Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 1-42 have been examined.

5. Claim 21 is objected to because of the following informalities: the preamble associates the limitations of the claim with “the system of claim 20”. As all previous claims, including claim 20, pertain to a method, the association is inappropriate. Examiner assumes the improper language was entered in error, and suggests changing the claim language to begin, “The method of claim 20”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 34 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 34 recites the limitation "the unique signatures" in line 1. There is insufficient antecedent basis for this limitation in the claim. It seems apparent to the examiner that the claim language misdirects the dependency of the claim towards claim 32.

As the "unique signatures" are introduced in claim 33, it is suggested that the language of claim 34 be changed to begin, "The system of claim 33, " and the examiner will assume dependence of claim 34 upon claim 33 in subsequent treatment of the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Ohguro et al, (U.S. 5,748,873).

Regarding claim 22, Ohguro teaches a computer system comprising:

- A primary processor and a secondary processor being configured to operate in lockstep, (see col. 1, lines 12-18); and
- An error-handling module to receive an error notification resulting from an error in either the primary processor or the secondary processor, (see col. 1, lines 48-50, and col. 2, lines 66-67), to determine if the error is a recoverable

error, (col. 3, lines 1-2), and, if the error is a recoverable error, then to initiate saving the state of either the primary or the secondary processor to a memory, (see col. 2, lines 63-66), and to reset and restart the primary and secondary processors using the saved state, (note col. 3, lines 1-8, and 29-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro as applied to claim 22 above, and further in view of Horst et al, (U.S. 6,233,702 B1).

Regarding claim 23, Ohguro teaches a system wherein the error handling module is configured to detect a divergence in the operation of the primary and secondary processors, (note col. 2, lines 63-66), and, as has been shown in reference to claim 22, is configured to receive an error notification from either of the processors.

Ohguro fails to teach a system wherein the error-handling module is further configured to receive a notification of a divergence in the operation of the primary and secondary processors before receiving the error notification, the error-handling module being further configured to:

- Wait for a predetermined time after receiving the notification of divergence; and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, to treat the error as a recoverable error.

However, Ohguro does teach performing a diagnosis program on the processors if a divergence is detected, to determine which processor is at fault, (see col. 1, lines 51-54).

Horst teaches a lockstep processing system, which is configured to receive a notification of a divergence in the operation of the primary and secondary processors before receiving an error notification, (see col. 77, lines 4-9), the error-handling module being further configured to:

- Wait for a predetermined time after receiving the notification of divergence, (col. 77, lines 55-59); and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, to treat the error as a recoverable error, (note col. 79, lines 12-25).

Horst and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the divergence handling teaching of Horst, with the divergence handling teaching of Ohguro, in order to achieve a divergence handling system which is capable of determining the cause of the divergence, utilizing the teachings of Horst, and, resultantly, determine whether an error can be treated as a recoverable error and what recovery operations are necessary to correct the error.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Horst meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. Horst states that, (see col. 77, lines 10-54), upon detecting a divergence in the operation of two lockstep processors, it is necessary to complete divergence handling in a short time period, in order to avoid transaction timeouts or unsupportable I/O delays. Thus, by providing a time period during which divergence handling must be completed, the teaching of Horst offers a distinct advantage over Ohguro. Also, Horst states that it is desirable to minimize disruption in the communication of the processing system, by permitting transmissions to continue in the event of a detected divergence, until a determination can be made as to which processor may be at fault. Once said

determination can be made, the teaching of Horst provides for disabling the faulty processor and continuing the transmission of non-faulty data. This provides a distinct advantage over the teaching of Ohguro, in improving the continuity of transmitted data in the face of a detected divergence. Therefore, one of ordinary skill in the art would have been motivated to utilize the divergence handling teaching of Horst to achieve said clearly recognized improvements in the lockstep processing system of Ohguro.

Regarding claim 31, Ohguro, in view of Horst, teaches a system, as described in reference to claim 23, further comprising a main memory, (see Ohguro, col. 2, lines 55-57), the system being configured to detect divergence by:

- Comparing memory commands generated by the primary processor with memory commands generated by the secondary processor, (note col. 15, lines 50-54, and 64-67; and col. 16, lines 1-6) ;
- Executing only the memory commands generated by the primary processor, (note col. 15, lines 64-67, and col. 16, lines 1-2); and
- Signaling a divergence detection if the memory commands issued by the primary processor differ form the memory commands issued by the secondary processor, (see col. 16, lines 4-6).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro et al as applied to claim 22 above, and further in view of Marshall et al, (U.S. 5,915,082).

Regarding claim 25, Ohguro fails to teach that non-recoverable error on the secondary processor is treated as a recoverable error. However, Ohguro does teach that the system is capable of continuing system operation in the event of a failure in either processor, (see col. 2, lines 35-40).

Marshall teaches a lockstep processor system in which an error, which would otherwise be determined a non-recoverable error, (see col. 5, lines 28-33), is treated as a recoverable error if the secondary processor determines that it has failed, (note col. 5, lines 35-38, and col. 6, lines 62-63).

Marshall and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant lockstep computer systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Marshall, to treat a non-recoverable error as a recoverable error in the system of Ohguro, in the case that said non-recoverable error is detected on the secondary processor.

One of ordinary skill in the art would have been motivated to combine the teachings because Marshall's solution satisfies a clearly recognized need in the art of lockstep computer systems, explicitly stated in Marshall. Marshall states that it is undesirable to stop a system's operation in the event of a non-recoverable error, (see col. 2, lines 31-35), and that high speed recovery is achieved, (note col. 2, line 58), in a system that treats a failure in a secondary processor as a recoverable error, by simply degrading the redundancy of the system. Therefore, one of ordinary skill would have been clearly motivated to combine the teachings as described above, in order to improve the rate of recovery from otherwise non-recoverable errors, supported by the fault-tolerant system of Ohguro.

10. Claims 1, 5, 11, 15, 16, 26, 32, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro as applied to claim 22 above, and further in view of Griffin et al, (U.S. 2002/0152418 A1).

Regarding claim 1, Ohguro teaches a method of error recover in a lockstep computer processing system, the system comprising a primary processor and a secondary processor, comprising the steps of:

- Operating the primary and secondary processors in lockstep, (see col. 1, lines 12-18);

- Receiving an error notification resulting from an error in either the primary processor or the secondary processor, (see col. 1, lines 48-50, and col. 2, lines 66-67);
- Determining if the error is a recoverable error, (col. 3, lines 1-2); and
- If the error is a recoverable error, then
    - Saving the state of either the primary or the secondary processor to a memory, (see col. 2, lines 63-66); and
    - Resetting and restarting the primary and secondary processors using the saved state, (note col. 3, lines 1-8, and 29-31).

Ohguro fails to teach that said system also comprises a bridge to a network. However, Ohguro does teach that said system comprises a bridge to I/O devices, (see col. 5, lines 63-64).

Griffin teaches a fault-tolerant, lockstep system comprising a bridge to a network, (note page 7, paragraph 0072, and page 1, paragraph 0006).

Griffin and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to substitute the bridge to a network, taught in Griffin, for the

I/O bridge taught in Ohguro, to achieve a method for a fault-tolerant system capable of communicating with a higher availability of resources.

One of ordinary skill in the art would have been motivated to substitute the network bridge of Griffin for the I/O bridge in Ohguro, because, as is explained in Griffin, paragraph 0072, said network bridge provides connection to a variety of external resources. One of ordinary skill in the art would have clearly recognized that it would be desirable to provide a computer system that communicates with external resources, such as the system of Ohguro, with the potential to communicate with a variety of external resources, in order to improve the availability of essential information and functionality.

Regarding claim 26, Ohguro fails to teach a system, as described in reference to claim 22, further comprising a bridge to a network, wherein, if the error is determined to be a non-recoverable error, then the system is configured to disable the bridge to the network before data corruption resulting from the error can propagate onto the network. However, Ohguro does teach that said system comprises a bridge to I/O devices, (see col. 5, lines 63-64), and that system resources are to be reset upon detection of a recoverable error.

Griffin teaches a fault-tolerant, lockstep system comprising a bridge to a network, (note page 7, paragraph 0072, and page 1, paragraph 0006), wherein detection of a non-recoverable results in a message to disable the bridge to the network, (see page 1, paragraph 0009), before data corruption resulting from the error can propagate onto the network.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the network connection and the step of disabling the bridge to the network, taught in Griffin, with the fault-tolerant system of Ohguro, in order to achieve a means of preventing the detected fault from propagating onto the network.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Griffin meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. Griffin states, (see page 1, paragraph 0002), that it is desirable that fault-tolerant systems comprise functionality to prevent far-reaching failures that can result when said systems are connected to a network. Therefore, one of ordinary skill in the art would have been motivated to disable the bridge to the I/O devices in Ohguro, in the event of a non-recoverable error, in order to prevent the error from affecting resources external to the fault-tolerant system.

Moreover, one of ordinary skill in the art would have been motivated to substitute the network bridge of Griffin for the I/O bridge in Ohguro, because, as is explained in Griffin, paragraph 0072, said network bridge provides connection to a variety of external resources. One of ordinary skill in the art would have clearly recognized that it would be desirable to provide a computer system that communicates with external resources, such as the system of Ohguro, with the potential to communicate with a variety of external resources, in order to improve the availability of essential information and functionality.

Claim 5 is rejected based on the arguments presented regarding claim 26, as it recites limitations similar to claim 26, except in the context of a method of error recovery.

Regarding claim 32, Ohguro fails to teach a computer system, as described in reference to claim 22, which comprises a bridge to an external network, and which is configured to:

- detect a divergence in the operation of the primary and secondary processors at the bridge to the network; and
- shut off the bridge to the network immediately unless the error has previously been determined to be a recoverable error.

However, Ohguro does teach detecting a divergence in the operation of the primary and secondary processors, (see col. 2, lines 63-66), and resetting the primary and secondary processors if the error causing said divergence is a recoverable error, (see col. 3, lines 1-8). It has also been shown above, in reference to claim 26, that one of ordinary skill in the art would have considered it obvious, and would have been motivated, to substitute the network bridge of Griffin for the I/O bridge in Ohguro.

Griffin teaches detecting a divergence between two lockstep processors at a network bridge, and shutting off the bridge to the network immediately as a result of a non-recoverable error, (see page 1, paragraphs 0006 and 0009).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the divergence detection of Griffin with the system of Ohguro, in order to achieve a fault-tolerant system that prevents an error from propagating externally in the event of a non-recoverable fault.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Griffin meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. In paragraph 0002, Griffin shows that it is critical, in fault-tolerant systems connected to a network, to prevent an error from propagating onto the network, and thus extensively effecting resources external to

the local system. The system of Ohguro is already capable of detecting a divergence between the operations of two lockstep processors, and resolving the associated error if said error is recoverable. The system of Ohguro fails, however, to explicitly disclose a means of handling a non-recoverable error, and of preventing a non-recoverable error from affecting external resources. Thus, the divergence checking system of Griffin offers a distinct advantage when combined with the system of Ohguro, by checking for divergence between processors at the network bridge, to indicate the potential for transmitting faulty data, and to allow the network bridge to prevent a non-recoverable fault from reaching beyond the local system. One of ordinary skill in the art would have been clearly motivated to combine the teachings in order to provide a means for handling non-recoverable errors in Ohguro, which ensures that errors do not affect resources external to the local system.

Claim 11 is rejected based on the arguments presented regarding claim 32, as it recites limitations similar to claim 32, except in the context of a method of error recovery.

Regarding claims 36 and 37, it has already been shown in reference to claims 22 and 32, that Ohguro, in view of Griffin, teaches a fault-tolerant system comprising a

bridge to an external network, wherein the processors are reset upon detecting a recoverable error. It is also implicit to the teachings that a reset of the processors includes a reset of the system comprising said processors, (note, Ohguro, col. 1, lines 66-67, and col. 2, line 1). Since computer processing operations inherently imply high-speed operations, the examiner determines that the teachings of Ohguro, in view of Griffin, comprise a system wherein the bridge is configured to conduct a high-speed reset and restart during the reset and restart of the primary and secondary processors. Moreover, it is inherent that a custom bridge, (as described in Griffin, paragraph 0072), would necessitate a custom high-speed reset and restart procedure.

Claims 15 and 16 are rejected based on the arguments presented regarding claims 36 and 37, as they recite limitations similar to claims 36 and 37, except in the context of a method of error recovery.

11. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro et al, as applied to claim 22 above, and further in view of Downing et al, (U.S. 4,589,090).

Regarding claim 27, Ohguro fails to teach that a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error. However, as has been shown, Ohguro does teach identifying and treating a hardware error as a recoverable error.

Downing teaches a multiprocessor system in which a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error, (see col. 6, lines 60-65).

Downing and Ohguro are analogous art because they are both from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fault tolerant system of Ohguro with the teachings of Downing, in order to achieve a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware component loss.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the system disclosed in Ohguro. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions

to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). Therefore, one of ordinary skill in the art would have been clearly motivated, in view of Downing, (see also, col. 6, lines 66-68, and col. 7, lines 1-2), to treat a hardware error, that results in the loss of non-essential system functions, as a recoverable error in order to allow primary system operations to proceed.

Regarding claim 28, Ohguro fails to teach that the error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical. However, Ohguro does teach that the error notification does distinguish between correctable and non-correctable faults, (see col. 7, lines 32-42).

Downing teaches a multiprocessor system in which an error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical, (see col. 7, lines 7-10).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fault tolerant system of Ohguro with the teachings of Downing, in order to achieve a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware

component loss. It is implicit that such a combination would also comprise Downing's teaching of using an error notification, that reports an error occurring in a hardware resource, including an identifier that can be used to determine whether the hardware resource is critical or non-critical.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the system disclosed in Ohguro. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). In order to enable a system to continue primary system functions in such an event, it is necessary that the error notification include an identifier that distinguishes between an error in a critical or non-critical hardware resource. Therefore, in view of Downing, one of ordinary skill in the art would have been motivated to include an error notification that reports an error occurring in a hardware resource, and identifies said error as occurring in either a critical or non-critical hardware resource, in the system disclosed in Ohguro, in order to enable said system to permit the continuation of primary system functions in the event of a non-essential resource failure.

Regarding claim 29, note Downing, col. 6, lines 66-68 and col. 7 lines 1-2, in which the hardware resource is ignored and effectively disabled.

Regarding claim 30, note col. 11, lines 44-50, in which the system is reset, and note col. 12, lines 19-21, in which the system is further configured to retry the hardware resource after processor restart to determine if the error in the hardware resource can be cured by a processor reset.

12. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Horst, as applied to claim 23 above, and further in view of Hofstee et al, (U.S. 6,751,749 B2).

Regarding claim 33, Ohguro, in view of Horst, fails to teach a system, as described in reference to claim 23, wherein the error-handling module does divergence detection by comparing unique signatures of processor state received from the primary and secondary processors. Though, as it has been shown, Ohguro, in view of Horst, does teach comparing the outputs of the two processors to detect a divergence.

Hofstee teaches a fault-tolerant, lockstep processing system, (note col. 2, lines 31-35), in which an error-handling module does divergence detection by comparing unique signatures of processor state received from primary and secondary processors, (see col. 2, lines 47-58).

Hofstee, Ohguro and Horst are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the comparing of signature for divergence detection, as taught in Hofstee, with the teachings of Ohguro, in view of Horst, in order to achieve an improved means of detecting divergence in the system of Ohguro, in view of Horst.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Hofstee meet a need, well known in the art, of providing a faster processing solution in systems, such as the fault-tolerant system of Ohguro, in view of Horst. Hofstee teaches that it is faster, and therefore advantageous, to check cumulative signatures at intervals rather than to check each individual result, (note col. 2, lines 56-58). One of ordinary skill in the art would have clearly recognized that the divergence checking of Ohguro, in view of Horst, by checking each output in order to detect a divergence, would be greatly improved by the

signature checking teachings of Hofstee. Therefore, one of ordinary skill in the art would have been motivated to combine said teachings, with the system of Ohguro, in view of Horst, in order to improve the processing speed in said system.

Regarding claim 34, it is inherent, though not explicitly stated, in the description of the signature generating teachings of Hofstee, described in reference to claim 33, that said unique signatures are generated by applying an algorithm to state information for the primary and secondary processors, (see, again, col. 2, lines 47-58)

13. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro as applied to claim 22 above, and further in view of Horrigan et al, (U.S. 6,658,532 B1).

Regarding claim 35, Ohguro teaches that the reset and restart of the primary and secondary processors includes the step of flushing the cache memory of either the primary or the secondary processor, (see col. 10, lines 12-20)

Ohguro fails to teach that said step of flushing the cache memory includes conducting first and second flushes of the cache memory.

Horrigan teaches a cache flushing operation comprising a first and second cache flush, (see col. 1, lines 14-17).

Horrigan and Ohguro are analogous art because they are from the same field of endeavor, viz., computer systems that improve reliability utilizing cache flush operations.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the staged cache flushing operation taught in Horrigan, with the cache flushing operation taught by Ohguro, to achieve an improved cache flushing operation during the reset and restart of the primary and secondary processors in the system of Ohguro.

One of ordinary skill in the art would have been motivated to combine the teachings because the cache flushing operation of Horrigan offers an explicitly stated advantage over the cache flushing operation of Ohguro. Horrigan states, (note col. 3, lines 1-16), that since interrupts cannot be serviced and a cache cannot be accessed during a cache flush, it is desirable to make the cache flush operation as fast as possible. By flushing the majority of the cache during the first stage, at a less critical time, and making the final flush brief, the flush can be immediately followed by a transition without significantly impacting the total duration between memory or

cache accesses. Therefore, one of ordinary skill in the art would have been properly motivated to combine the teachings in order to reduce the time before interrupts and cache accesses are enabled, following a cache flush.

14. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro as applied to claim 22 above, and further in view of Burdett et al, (U.S. 6,327,675 B1).

Regarding claim 38, Ohguro fails to teach that the system, described in reference to claim 22, further comprises a watchdog timer, the system treating the error as a non-recoverable error if the watchdog timer expires during the reset and restart of the primary and secondary processors. However, Ohguro does teach some means for determining whether a fault is recoverable, and resetting the primary and secondary processors in the event of a fault, (see col. 3, lines 33-37, and col. 2, lines 60-63).

Burdett teaches a fault-tolerant, multiprocessor system in which an error is detected, and the error is treated as a non-recoverable error if a watchdog timer expires during the reset and restart of the primary processor, (see col. 1, lines 36-48, and col. 2 lines 12-14).

Burdett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the watchdog timer of Burdett with the fault-tolerant system of Ohguro in order to achieve a means of determining whether a fault detected by either the primary or secondary processor is recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the watchdog timer taught in Burdett meets an explicitly stated need of Ohguro. Ohguro teaches that a fault detected by either the primary or secondary processor should be determined to be recoverable or non-recoverable. Moreover, Ohguro shows that, in the event of such a fault, the primary and secondary processors are to be reset as a means of attempting to correct the fault. Burdett teaches that when a processor is reset in attempt to correct a fault, a non-recoverable error is indicated when said processor is unable to restart before the expiration of a watchdog timer. By combining the watchdog timer taught in Burdett with the fault-tolerant system taught in Ohguro, the system of Ohguro is capable of correcting a recoverable error by a system reset, and indicating a non-recoverable error when such a correction is not possible, thus meeting the need expressed in Ohguro.

15. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro in view of Burdett, as applied to claim 38 above, and further in view of Davis, (U.S. 5,345,583).

Ohguro, in view of Burdett, fails to teach a system as described in reference to claim 38, wherein the system conducts a hard-reset of the lockstep computer processing system upon expiry of the watchdog timer. However, Ohguro, in view of Burdett, does teach that the expiry of the watchdog timer indicates that the previous reset was incapable of correcting an error determined to be non-recoverable.

Davis teaches a fault-tolerant system in which a hard-reset is conducted when other resets are incapable of correcting a fault condition, (see col. 5, lines 48-58, and col. 6, lines 15-20).

Davis, Ohguro and Burdett are analogous art because they are all from the same field of endeavor, viz., fault-tolerant processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings of Davis with the fault-tolerant system of Ohguro, in view of Burdett, in order to achieve an automatic means of attempting to correct a system error that is otherwise determined to be non-recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the hard-reset of Davis meets an implicit need of Ohguro, in view of Burdett. It would have been clearly recognized by one of ordinary skill in the art, in view of Ohguro, and further in view of Burdett, that it is desirable in fault-tolerant systems to quickly and automatically resolve system errors, in order to allow system functions to proceed without human intervention. The system of Ohguro, in view of Burdett, treats an error as a non-recoverable error in the event that a watchdog timer expires before a faulty processor is capable of restarting. As it is always desirable in fault-tolerant systems to provide an automatic solution to a fault condition, one of ordinary skill in the art would have been clearly motivated to combine the hard-reset taught in Davis, with the system of Ohguro, in view of Burdett, in order to achieve a means of automatically correcting an otherwise non-recoverable error.

16. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, as applied to claim 1 above, and further in view of Horst.

Regarding claim 2, Ohguro, in view of Griffin, teaches a method comprising the steps of detecting a divergence in the operation of the primary and secondary processors, (note col. 2, lines 63-66), and, as has been shown in reference to claim 22, is configured to receive an error notification from either of the processors.

Ohguro, in view of Griffin, fails to teach a method comprising the steps of:

- Detecting a divergence in the operation of the primary and secondary processors before receiving the error notification;
- Waiting for a predetermined time after detecting the divergence; and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, then treating the error as a recoverable error.

However, Ohguro does teach performing a diagnosis program on the processors if a divergence is detected, to determine which processor is at fault, (see col. 1, lines 51-54).

Horst teaches a method for a lockstep processing system, comprising the steps of:

- Detecting a notification of a divergence in the operation of the primary and secondary processors before receiving an error notification, (see col. 77, lines 4-9);
- Waiting for a predetermined time after detecting the divergence, (col. 77, lines 55-59); and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, then treating the error as a recoverable error, (note col. 79, lines 12-25).

Horst, Griffin and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the divergence handling teaching of Horst, with the divergence handling teaching of Ohguro, in view of Griffin, in order to achieve a divergence handling system which is capable of determining the cause of the divergence, utilizing the teachings of Horst, and, resultantly, determine whether an error can be treated as a recoverable error and what recovery operations are necessary to correct the error.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Horst meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. Horst states that, (see col. 77, lines 10-54), upon detecting a divergence in the operation of two lockstep processors, it is necessary to complete divergence handling in a short time period, in order to avoid transaction timeouts or unsupportable I/O delays. Thus, by providing a time period during which divergence handling must be completed, the teaching of Horst offers a distinct advantage over Ohguro, in view of Griffin. Also, Horst states that it is desirable to minimize disruption in the communication of the processing system, by permitting transmissions to continue in the event of a detected divergence, until a determination can be made as to which processor may be at fault. Once said

determination can be made, the teaching of Horst provides for disabling the faulty processor and continuing the transmission of non-faulty data. This provides a distinct advantage over the teaching of Ohguro, in view of Griffin, in improving the continuity of transmitted data in the face of a detected divergence. Therefore, one of ordinary skill in the art would have been motivated to utilize the divergence handling teaching of Horst to achieve said clearly recognized improvements in the lockstep processing system of Ohguro, in view of Griffin.

Regarding claim 10, Ohguro, in view of Griffin and Horst, teaches a method for a system, as described in reference to claim 2, that includes a main memory, (see Ohguro, col. 2, lines 55-57), the step of detecting divergence comprises the steps of:

- Comparing memory commands generated by the primary processor with memory commands generated by the secondary processor, (note col. 15, lines 50-54, and 64-67; and col. 16, lines 1-6) ;
- Executing only the memory commands generated by the primary processor, (note col. 15, lines 64-67, and col. 16, lines 1-2); and
- Signaling a divergence detection if the memory commands issued by the primary processor differ form the memory commands issued by the secondary processor, (see col. 16, lines 4-6).

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, as applied to claim 1 above, and further in view of Marshall.

Regarding claim 4, Ohguro, in view of Griffin, fails to teach that non-recoverable error on the secondary processor is treated as a recoverable error. However, Ohguro, in view of Griffin, does teach that the method is capable of continuing system operation in the event of a failure in either processor, (see col. 2, lines 35-40).

Marshall teaches a method for a lockstep processor system in which an error, which would otherwise be determined a non-recoverable error, (see col. 5, lines 28-33), is treated as a recoverable error if the secondary processor determines that it has failed, (note col. 5, lines 35-38, and col. 6, lines 62-63).

Marshall, Griffin, and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep computer systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Marshall, to treat a non-recoverable error as a recoverable error in the method of Ohguro, in view of Griffin, in the case that said non-recoverable error is detected on the secondary processor.

One of ordinary skill in the art would have been motivated to combine the teachings because Marshall's solution satisfies a clearly recognized need in the art of lockstep computer systems, explicitly stated in Marshall. Marshall states that it is undesirable to stop a system's operation in the event of a non-recoverable error, (see col. 2, lines 31-35), and that high speed recovery is achieved, (note col. 2, line 58), in a system that treats a failure in a secondary processor as a recoverable error, by simply degrading the redundancy of the system. Therefore, one of ordinary skill would have been clearly motivated to combine the teachings as described above, in order to improve the rate of recovery from otherwise non-recoverable errors, supported by the fault-tolerant method of Ohguro, in view of Griffin.

18. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro,I in view of Griffin, as applied to claim 1 above, and further in view of Downing.

Regarding claim 6, Ohguro, in view of Griffin, fails to teach that a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error. However, as has been shown, Ohguro does teach identifying and treating a hardware error as a recoverable error.

Downing teaches a method for a multiprocessor system in which a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error, (see col. 6, lines 60-65).

Downing, Griffin, and Ohguro are analogous art because they are both from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fault tolerant system of Ohguro, in view of Griffin, with the teachings of Downing, in order to achieve a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware component loss.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the system disclosed in Ohguro, in view of Griffin. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). Therefore, one of ordinary skill in the art would have been clearly motivated, in view of Downing, (see also, col. 6, lines 66-68, and col. 7, lines 1-2), to treat a hardware error, that results in the loss of non-

essential system functions, as a recoverable error in order to allow primary system operations to proceed.

Regarding claim 7, Ohguro, in view of Griffin, fails to teach that the error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical. However, Ohguro, in view of Griffin, does teach that the error notification does distinguish between correctable and non-correctable faults, (see col. 7, lines 32-42).

Downing teaches a method for a multiprocessor system in which an error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical, (see col. 7, lines 7-10).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the method for a fault tolerant system of Ohguro, in view of Griffin, with the teachings of Downing, in order to achieve a method for a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware component loss. It is implicit that such a combination would also comprise Downing's teaching of using an error notification,

that reports an error occurring in a hardware resource, including an identifier that can be used to determine whether the hardware resource is critical or non-critical.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the method disclosed in Ohguro, in view of Griffin. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). In order to enable a system to continue primary system functions in such an event, it is necessary that the error notification include an identifier that distinguishes between an error in a critical or non-critical hardware resource. Therefore, in view of Downing, one of ordinary skill in the art would have been motivated to include an error notification that reports an error occurring in a hardware resource, and identifies said error as occurring in either a critical or non-critical hardware resource, in the method disclosed in Ohguro, in view of Griffin, in order to enable said method to permit the continuation of primary system functions in the event of a non-essential resource failure.

Regarding claim 8, note Downing, col. 6, lines 66-68 and col. 7 lines 1-2, in which the hardware resource is ignored and effectively disabled.

Regarding claim 9, note col. 11, lines 44-50, in which the system is reset, and note col. 12, lines 19-21, in which the system is further configured to retry the hardware resource after processor restart to determine if the error in the hardware resource can be cured by a processor reset..

19. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Horst, as applied to claim 2 above, and further in view of Hofstee.

Regarding claim 12, Ohguro, in view of Griffin and Horst, fails to teach a method, as described in reference to claim 2, wherein the divergence detection is conducted by comparing unique signatures of processor state received from the primary and secondary processors. Though, as it has been shown, Ohguro, in view of Griffin and Horst, does teach comparing the outputs of the two processors to detect a divergence.

Hofstee teaches a fault-tolerant, lockstep processing method, (note col. 2, lines 31-35), in which divergence detection is conducted by comparing unique signatures of processor state received from primary and secondary processors, (see col. 2, lines 47-58).

Hofstee, Griffin, Ohguro and Horst are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the comparing of signature for divergence detection, as taught in Hofstee, with the teachings of Ohguro, in view of Griffin and Horst, in order to achieve an improved means of detecting divergence in the method of Ohguro, in view of Griffin and Horst.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Hofstee meet a need, well known in the art, of providing a faster processing solution in methods, such as the fault-tolerant method of Ohguro, in view of Griffin and Horst. Hofstee teaches that it is faster, and therefore advantageous, to check cumulative signatures at intervals rather than to check each individual result, (note col. 2, lines 56-58). One of ordinary skill in the art would have clearly recognized that the divergence checking of Ohguro, in view of Griffin and Horst, by checking each output in order to detect a divergence, would be greatly improved by the signature checking teachings of Hofstee. Therefore, one of ordinary skill in the art would have been motivated to combine said teachings, with the system of Ohguro, in view of Griffin and Horst, in order to improve the processing speed in said system.

Regarding claim 13, it is inherent, though not explicitly stated, in the description of the signature generating teachings of Hofstee, described in reference to claim 12, that said unique signatures are generated by applying an algorithm to state information for the primary and secondary processors, (see, again, col. 2, lines 47-58)

20. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, as applied to claim 1 above, and further in view of Horrigan.

Regarding claim 14, Ohguro, in view of Griffin, teaches that method, described in reference to claim 1, includes the step of flushing the cache memory of either the primary or the secondary processor, (see col. 10, lines 12-20)

Ohguro, in view of Griffin, fails to teach that said step of flushing the cache memory includes conducting first and second flushes of the cache memory.

Horrigan teaches a cache flushing operation comprising a first and second cache flush, (see col. 1, lines 14-17).

Horrigan, Griffin, and Ohguro are analogous art because they are from the same field of endeavor, viz., computer systems that improve reliability utilizing cache flush operations.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the staged cache flushing operation taught in Horrigan, with the cache flushing operation taught by Ohguro, in view of Griffin, to achieve an improved cache flushing operation during the reset and restart of the primary and secondary processors in the system of Ohguro, in view of Griffin.

One of ordinary skill in the art would have been motivated to combine the teachings because the cache flushing operation of Horrigan offers an explicitly stated advantage over the cache flushing operation of Ohguro, in view of Griffin. Horrigan states, (note col. 3, lines 1-16), that since interrupts cannot be serviced and a cache cannot be accessed during a cache flush, it is desirable to make the cache flush operation as fast as possible. By flushing the majority of the cache during the first stage, at a less critical time, and making the final flush brief, the flush can be immediately followed by a transition without significantly impacting the total duration between memory or cache accesses. Therefore, one of ordinary skill in the art would have been properly motivated to combine the teachings in order to reduce the time before interrupts and cache accesses are enabled, following a cache flush in the method of Ohguro, in view of Griffin.

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, as applied to claim 1 above, and further in view of Burdett.

Regarding claim 17, Ohguro, in view of Griffin, fails to teach that the method, described in reference to claim 1, further comprises the steps of setting a watchdog timer, the system treating the error as a non-recoverable error if the watchdog timer expires before the resetting of the primary and secondary processors. However, Ohguro, in view of Griffin, does teach some means for determining whether a fault is recoverable, and resetting the primary and secondary processors in the event of a fault, (see, Ohguro, col. 3, lines 33-37, and col. 2, lines 60-63).

Burdett teaches a method for a fault-tolerant, multiprocessor system in which an error is detected, and the error is treated as a non-recoverable error if a watchdog timer expires before the resetting of the primary processor, (see col. 1, lines 36-48, and col. 2 lines 12-14).

Burdett, Griffin and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the watchdog timer of Burdett with the method of Ohguro, in view of Griffin, in order to achieve a means of determining whether a fault detected by either the primary or secondary processor is recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the watchdog timer taught in Burdett meets an explicitly stated need of Ohguro, in view of Griffin. Ohguro, in view of Griffin, teaches that a fault detected by either the primary or secondary processor should be determined to be recoverable or non-recoverable. Moreover, Ohguro, in view of Griffin, shows that, in the event of such a fault, the primary and secondary processors are to be reset as a means of attempting to correct the fault. Burdett teaches that when a processor is reset in attempt to correct a fault, a non-recoverable error is indicated when said processor is unable to restart before the expiration of a watchdog timer. By combining the watchdog timer taught in Burdett with the fault-tolerant method taught in Ohguro, in view of Griffin, the method of Ohguro, in view of Griffin, is capable of correcting a recoverable error by a system reset, and indicating a non-recoverable error when such a correction is not possible, thus meeting the need expressed in Ohguro, in view of Griffin.

22. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro in view of Griffin and Burdett, as applied to claim 17 above, and further in view of Davis.

Ohguro, in view of Griffin and Burdett, fails to teach a method as described in reference to claim 17, wherein the step of treating the error as a non-recoverable error comprises the step of conducting a hard-reset of the lockstep computer processing system. However, Ohguro, in view of Griffin and Burdett, does teach that the expiry of the watchdog timer indicates that the previous reset was incapable of correcting an error determined to be non-recoverable.

Davis teaches a method for fault-tolerant system in which a hard-reset is conducted when other resets are incapable of correcting a fault condition, (see col. 5, lines 48-58, and col. 6, lines 15-20).

Davis, Griffin, Ohguro and Burdett are analogous art because they are all from the same field of endeavor, viz., fault-tolerant processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings of Davis with the fault-tolerant method of Ohguro, in view of Griffin and Burdett, in order to achieve an automatic

means of attempting to correct a system error that is otherwise determined to be non-recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the hard-reset of Davis meets an implicit need of Ohguro, in view of Griffin and Burdett. It would have been clearly recognized by one of ordinary skill in the art, in view of Ohguro, and further in view of Griffin and Burdett, that it is desirable in fault-tolerant systems to quickly and automatically resolve system errors, in order to allow system functions to proceed without human intervention. The method of Ohguro, in view of Griffin and Burdett, treats an error as a non-recoverable error in the event that a watchdog timer expires before a faulty processor is capable of restarting. As it is always desirable in fault-tolerant systems to provide an automatic solution to a fault condition, one of ordinary skill in the art would have been clearly motivated to combine the hard-reset taught in Davis, with the method of Ohguro, in view of Griffin and Burdett, in order to achieve a means of automatically correcting an otherwise non-recoverable error.

Allowable Subject Matter

23. Claims 3, 19-21, 24 and 40-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3 and 24, the limitation, "if the error notification is received after the expiry of the predetermined time, then treating the error as a non-recoverable error," in combination with the other limitations of the claims was not found in any prior art.

Regarding claims 19 and 40, the limitation of, "running the bridge to the network from a main memory until a bridge local memory has been initialized upon the reset and restart of the primary and secondary processors," in combination with the other limitations of the claims was not found in any prior art.

Regarding claims 20 and 41, the limitation of, "sending a data message to the network bridge over the network, and, when the data message is lost due to the resetting and restarting of the primary and secondary processors, to:

- Send a first inquiry message to the network bridge after a first timeout period, and, when the first inquiry message is lost, to:
- Send a second inquiry message after a second timeout period;

Wherein the sum of the first and second timeout periods is selected to be greater than an expected recovery time for the primary and secondary processors," in combination with the other limitations of the claim was not found in any prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (703) 605-1211, or (571) 272-3662 after Oct. 15, 2004 . The examiner can normally be reached on Mon-Fri, from 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713, or (571) 272-3645 after Oct. 15, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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